PRELIMINARY

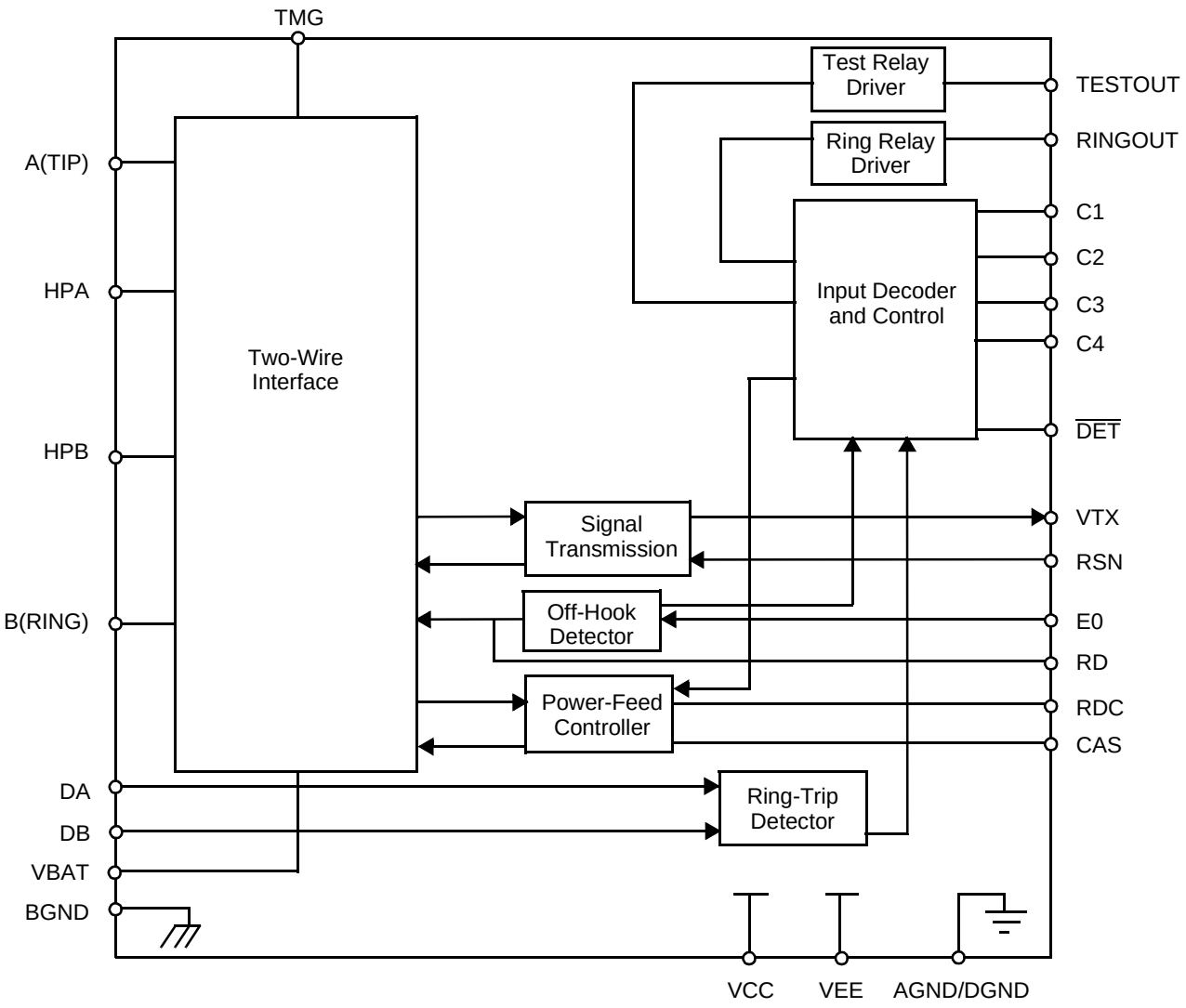
Am7947

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Ideal for China National applications**
- **Low standby power**
- **–39.8 V to –58 V battery operation**
- **On-hook transmission**
- **Tip Open state for ground-start lines**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Current gain = 200**
- **Polarity reversal option**
- **On-chip Thermal Management (TMG) feature**
- **On-chip ring and test relay driver and relay snubber circuits**

BLOCK DIAGRAM



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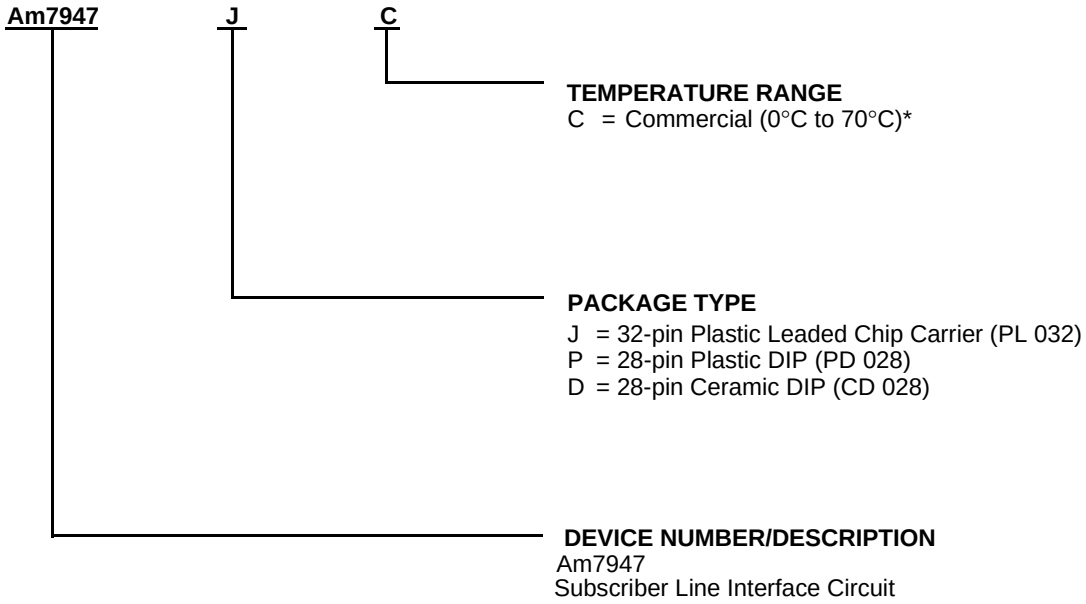
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am7947	JC PC DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

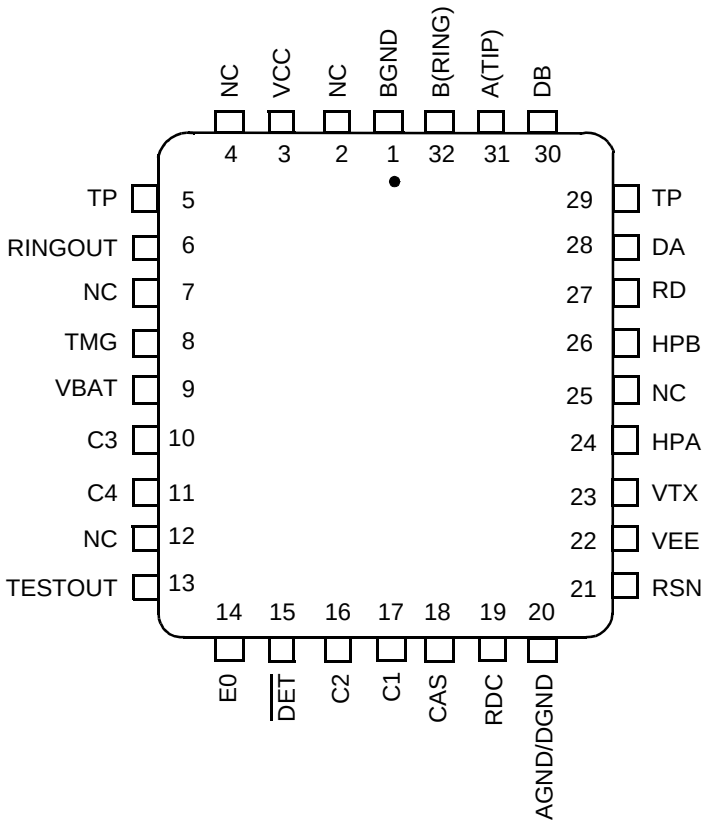
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

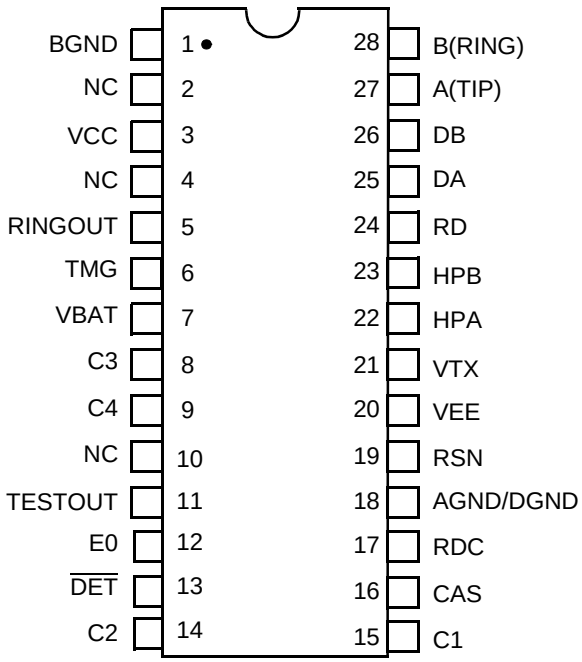
CONNECTION DIAGRAMS

Top View

32-Pin PLCC



28-Pin Plastic or Ceramic DIP



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *NC = No Connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C4–C1	Input	Decoder. TTL compatible. C4 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E0). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	$\overline{\text{DET}}$ Enable. A logic High disables $\overline{\text{DET}}$. A logic Low enables $\overline{\text{DET}}$.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. This pin not internally connected.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TESTOUT	Output	Test Relay Driver. Open collector driver with emitter internally connected to AGND.
TMG	Thermal	Thermal Management. External resistor connects between this pin and VBAT to offload power dissipation from SLIC. Functions during normal polarity, Active state.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND ..... –0.4 V to +7 V

V_{EE} with respect to AGND/DGND..... +0.4 V to –7 V

V_{BAT} with respect to AGND/DGND:

Continuous..... +0.4 V to –70 V

10 ms ..... +0.4 V to –75 V

BGND with respect to AGND/DGND..... +3 V to –3 V

A(TIP) or B(RING) to BGND:

Continuous ..... –70 V to +1 V

10 ms (f = 0.1 Hz) ..... –70 V to +5 V

1 µs (f = 0.1 Hz) ..... –80 V to +8 V

250 ns (f = 0.1 Hz) ..... –90 V to +12 V

Current from A(TIP) or B(RING).....±150 mA

RINGOUT/TESTOUT current .....50 mA

RINGOUT/TESTOUT voltage ..... BGND to +7 V

RINGOUT/TESTOUT transient..... BGND to +10 V

DA and DB inputs

Voltage on ring-trip inputs.....V_{BAT} to 0 V

Current into ring-trip inputs.....±10 mA

C4–C1 and E0

Input voltage .....–0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous, T_A = 70°C, No heat sink (See note):

In 32-pin PLCC package.....1.7 W

In 28-pin ceramic DIP package.....2.5 W

In 28-pin plastic DIP package .....1.4 W

Thermal Data..... θ_{JA}

In 32-pin PLCC package.....43°C/W typ

In 28-pin ceramic DIP package.....30°C/W typ

In 28-pin plastic DIP package .....53°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature..... 0°C to +70°C*

V_{CC} .....4.75 V to 5.25 V

V_{EE} .....–4.75 V to –5.25 V

V_{BAT} .....–38.9 V to –58 V

AGND/DGND..... 0 V

BGND with respect to AGND/DGND .....–100 mV to +100 mV

Load resistance on VTX to ground..... 10 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4, 7
Analog output (V_{TX}) impedance			3		W	4
Analog (V_{TX}) output offset voltage	0°C to +70°C –40°C to +85°C	–40 –45		+40 +45	mV	— 4
Overload level, 2-wire and 4-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.9			Vrms	2b
THD (Total Harmonic Distortion)	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, on hook	0 dBm, R_L = 600 Ω			–35.5		
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic L-T, L-4	200 Hz to 3.4 kHz 0°C to +70°C –40°C to +85°C	 52 50	 70		dB	 — 4
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity	40				
Longitudinal current per pin	Active state OHT state	20 10	35 17.5		mArms	
Longitudinal impedance at A or B	0 to 100 Hz		25	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω		+7	+14	dBrnC	4
Psophometric weighted noise	R_L = 600 Ω		–83	–76	dBmp	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	 –0.15 –0.20		 +0.15 +0.20	dB	 — 4
Gain accuracy over frequency	300 Hz to 3400 Hz 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		 5 4
Gain tracking relative to 0 dBm	+3 dBm to –55 dBm 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		 4 4
Gain accuracy	On-hook, OHT state	–1.0		+1.0		4
Balance Return Signal (4- to 4-Wire)						
Gain accuracy over temperature	Ref: 0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	 –0.15 –0.20		 +0.15 +0.20	dB	 3 4
Gain accuracy over frequency	300 Hz to 3400 Hz 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		 3 4
Gain tracking relative to 0 dBm	+3 dBm to –55 dBm 0°C to +70°C –40°C to +85°C	 –0.1 –0.15		 +0.1 +0.15		 3, 4 4
Group delay	0 dBm, 1 kHz		4		µs	4, 7

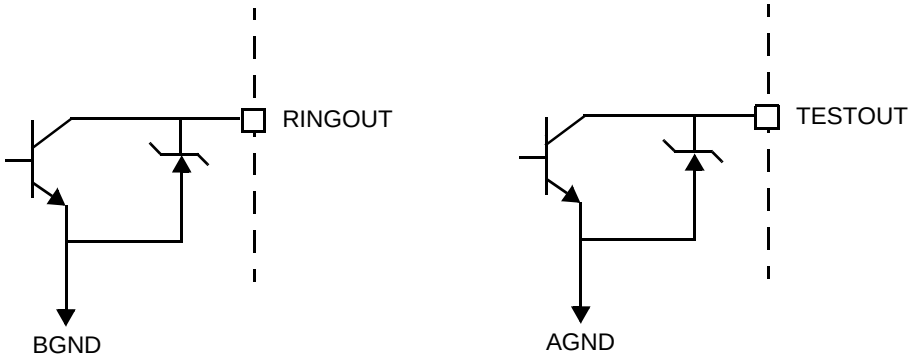
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Short loops, Active or OHT	R_{LDC} = 600 Ω 0°C to +70°C –40°C to +85°C	20 19.8	22 22	24 24	mA	— 4
I_L, Long loops, Active or OHT	R_{LDC} = 600 Ω, BAT = 39.8 V	18	18.6		mA	
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	0.7I_L	I_L	1.3I_L	mA	
	R_L = 600 Ω	13	18.7		mA	
I_L, Loop current, Tip Open state	R_L = 0 Ω B to GND B to V_{BAT} +6 V		0 30 30	100	µA mA mA	
I_L, Loop current, Open Circuit state	R_L = 0 Ω			100	µA	
I_LLIM	Active, A and B to GND		100	130	mA	
V_A, Active, ground-start signaling	A to –48 V = 7 Ω, B to GND = 100 Ω	–7.5	–5			4
V_{AB}, Open circuit voltage		–40	–42		V	
Power Supply Rejection Ration (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3.4 kHz	30	40		dB	5
V_{EE}	50 Hz to 3.4 kHz	28	35		dB	5
V_{BAT}	50 Hz to 3.4 kHz	28	50		dB	5
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
Power Dissipation						
On hook, Open Circuit state			25	100	mW	
On hook, Standby state			45	85	mW	
On hook, OHT state			120	180	mW	
On hook, Active state	R_{TMG} = Open R_{TMG} = 2 kΩ		180 195	270 300	mW	
Off hook, Standby state	R_L = 600 Ω		860	1300	mW	
Off hook, OHT state	R_{TMG} = Open, R_L = 300 Ω		1000	1400	mW	
Off hook, Active state	R_{TMG} = 2 kΩ, R_L = 300 Ω		450	800	mW	
Supply Currents, Battery = –58 V						
I_{CC}, on-hook V_{CC} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		1.7 4.9 2.2 6.3	2.5 7.5 3.0 8.5	mA	
I_{EE}, on-hook V_{EE} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0	mA	
I_{BAT}, on-hook V_{BAT} supply current	Open Circuit state OHT state Standby state Active state, BAT = –48 V		0.18 0.19 0.45 4.2	1.0 4.7 1.5 5.7	mA	
RFI Rejection						
RFI rejection	100 kHz to 30 MHz (See Figure F)			1.0	mVrms	4

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Inputs (C4–C1 and E0)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage						
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current	C4–C1 and E0	–400				
Logic Output ($\overline{DET}$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.4	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Loop Detector						
IT, Loop-detect threshold tolerance	R_D = 35.4 kΩ, $I_T = 375/R_D$	–12		12	%	
Relay Driver Output (RINGOUT)						
On voltage	I_{OL} = 35 mA		+0.3	+0.5	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener on voltage	I_Z = 30 mA		10			
Test Driver Output (TESTOUT)						
On voltage	I_{OL} = 35 mA		+0.5	+0.75	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener on voltage	I_Z = 30 mA		10			

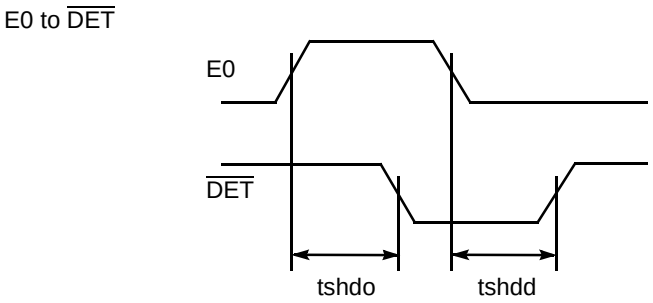
RELAY DRIVER SCHEMATICS



SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tshdd	E0 Low to $\overline{DET}$ Low	Switchhoook Detect State (See Figure E)	0°C to +70°C –40°C to 85°C			1.1 1.6	µs	4
tshdo	E0 Low to $\overline{DET}$ High					3.8 4.0		

SWITCHING WAVEFORMS

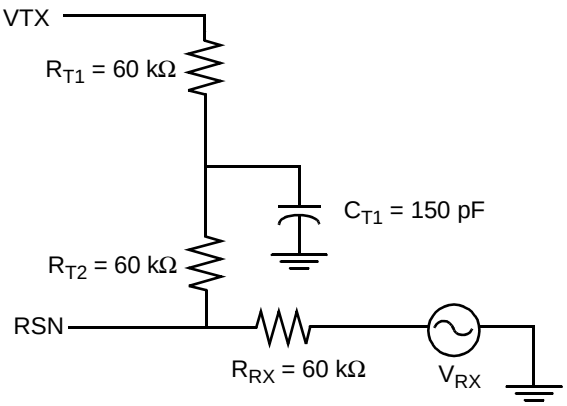


Note:

All delays measured at 1.4 V level.

Notes:

1. *Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 11.36 kΩ, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.33 µF, C_{DC} = 0.33 µF, C_{CAS} = 0.33 µF, D_1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs. The effect of group delay on the linecard performance may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

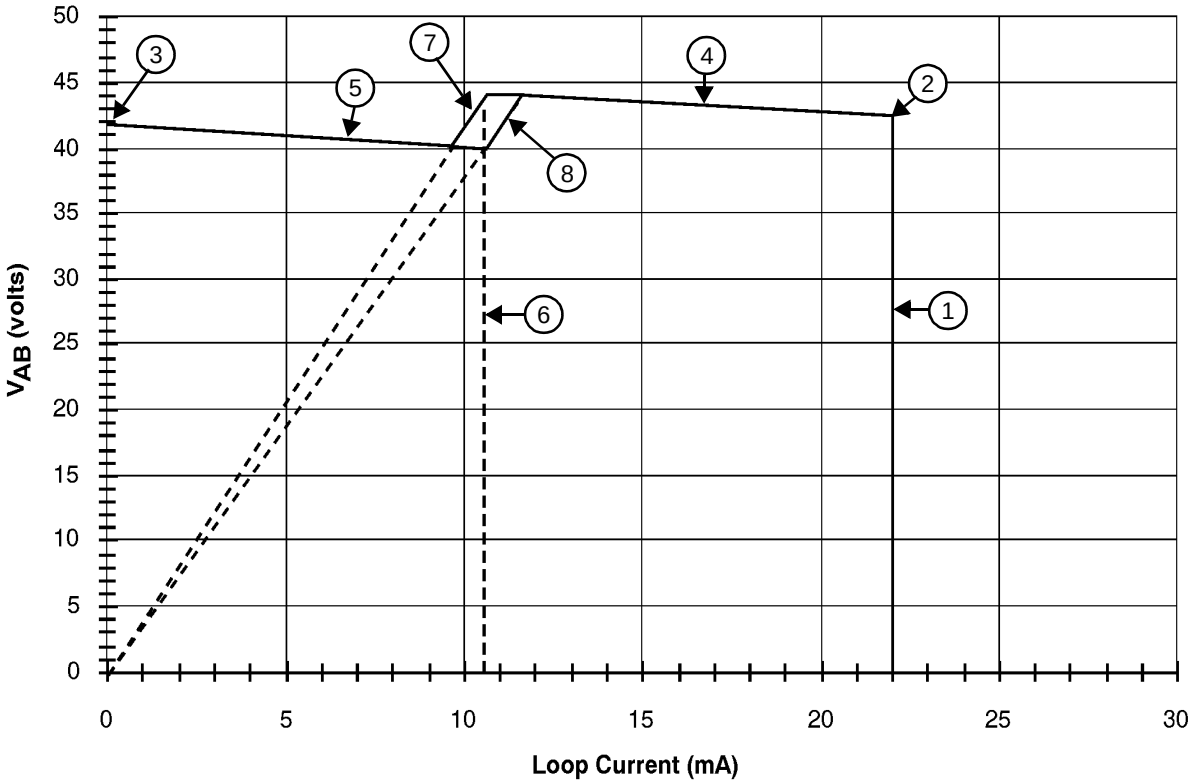
State	C3	C2	C1	Two-Wire Status	$\overline{\text{DET}}$ Output
0	0	0	0	Open Circuit	Ring trip
1	0	0	1	Ringing	Ring trip
2	0	1	0	Active	Loop detector
3	0	1	1	On-hook TX (OHT)	Loop detector
4	1	0	0	Tip Open	Loop detector
5	1	0	1	Standby	Loop detector
6	1	1	0	Active Polarity Reversal	Loop detector
7	1	1	1	OHT Polarity Reversal	Loop detector

Note:
C4 logic High enables the TESTOUT relay driver.

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}, \quad C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{OHT} = \frac{500}{R_{DC1} + R_{DC2}}$	OHT loop current (constant-current region).
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{V_{BAT} - 6\ \text{V}}{I_{LOOP}}$	R_{TMG} is connected from TMG to VBAT and is used to limit power dissipation within the SLIC in Normal Active and Tip Open states only.
$P_{RTMG} = \frac{(V_{BAT} - 6\ \text{V} - (I_L \bullet R_L))^2}{R_{TMG}}$	Power dissipated in the thermal management resistor, R_{TMG}, during Active and Tip Open states.
$P_{SLIC} = V_{BAT} \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ \text{W}$	Power dissipated in the SLIC while in Active and Tip Open states.

DC FEED CHARACTERISTICS



R_{DC} = 22.72 kΩ
V_{BAT} = 48 V
R_D = 35.4 kΩ

Active state
OHT state

Notes:

1. *Constant-current region:* $I_L = \frac{500}{R_{DC}}$

2. *Anti-sat (battery tracking) turn-on:*
$V_{AB} = 1.053\,|V_{BAT}| - 6.43, \quad |V_{BAT}| < 39.5\ V$
$V_{AB} = 0.842\,|V_{BAT}| + 1.9, \quad |V_{BAT}| \geq 39.5\ V$

3. *Open Circuit voltage:*
$V_{AB} = 1.053\,|V_{BAT}| - 7.08, \quad |V_{BAT}| < 39.5\ V$
$V_{AB} = 0.842\,|V_{BAT}| + 1.25, \quad |V_{BAT}| \geq 39.5\ V$

4. *Anti-sat region ($I_L > I_{DET}$):*
$V_{AB} = 1.053|V_{BAT}| - 6.43 + \frac{500}{120} - I_L \bullet \frac{R_{DC}}{120}, \quad |V_{BAT}| < 39.5\ V$
$V_{AB} = 0.842|V_{BAT}| + 1.9 + \frac{500}{150} - I_L \bullet \frac{R_{DC}}{150}, \quad |V_{BAT}| \geq 39.5\ V$

5. *Anti-sat region ($I_L < I_{DET}$):*
$V_{AB} = 1.053|V_{BAT}| - 7.08 - I_L \bullet \frac{R_{DC}}{120}, \quad |V_{BAT}| < 39.5\ V$
$V_{AB} = 0.842|V_{BAT}| + 1.25 - I_L \bullet \frac{R_{DC}}{150}, \quad |V_{BAT}| \geq 39.5\ V$

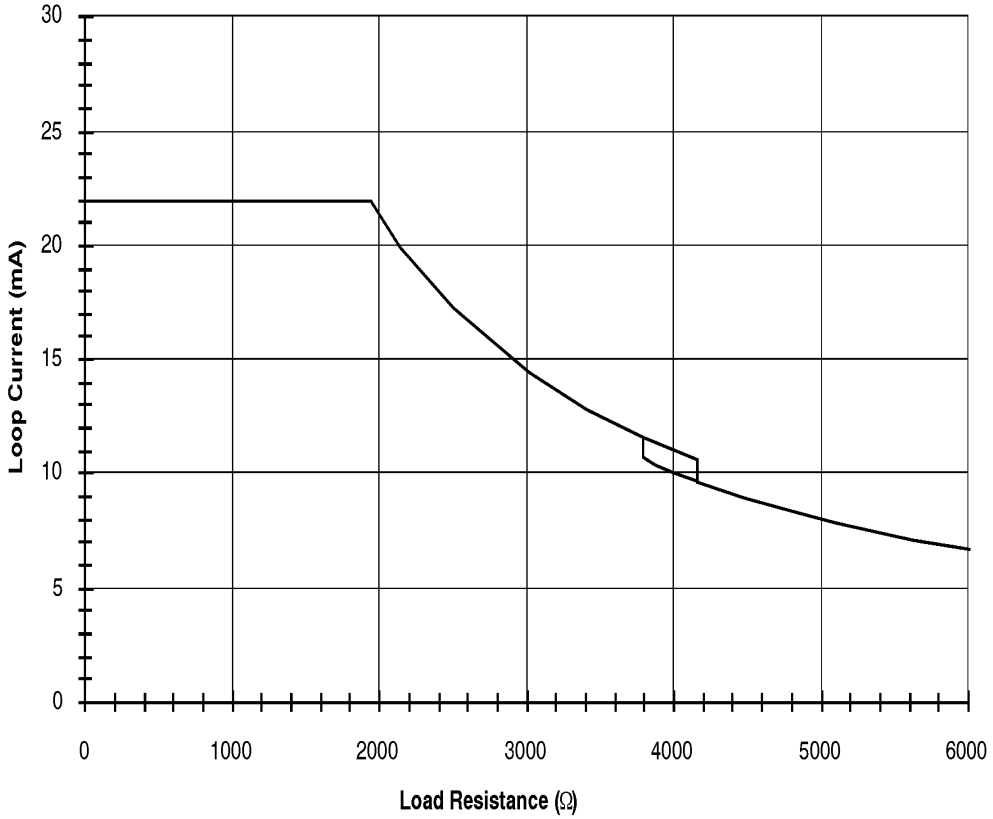
6. *Loop-detect threshold (I_{DET}):* $I_{DET} = \frac{375}{R_{DC}}$

7. *Anti-sat transition region, off-hook to on-hook.*

8. *Anti-sat transition region, on-hook to off-hook.*

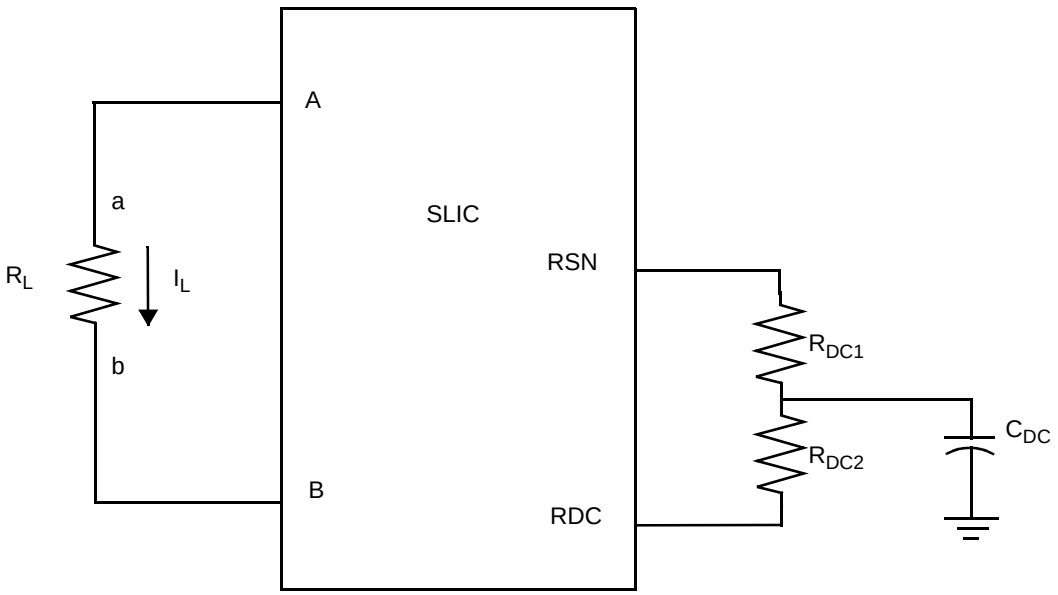
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



R_{DC} = 22.72 kΩ
V_{BAT} = 48 V
R_D = 35.4 kΩ

b. Loop Current vs. Load Resistance (Typical)

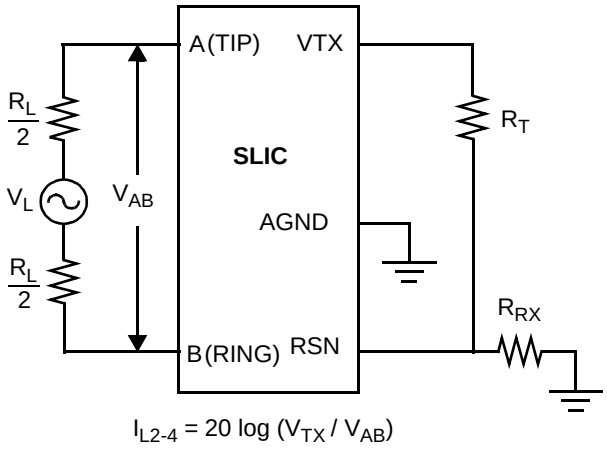


Feed current programmed by R_{DC1} and R_{DC2}

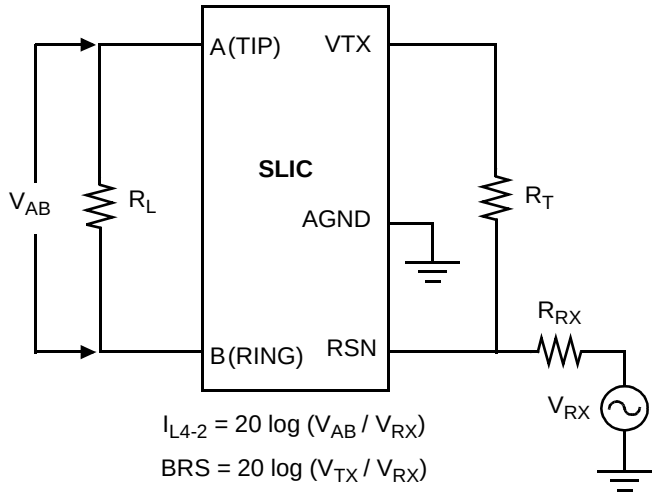
c. Feed Programming

Figure 1. DC Feed Characteristics

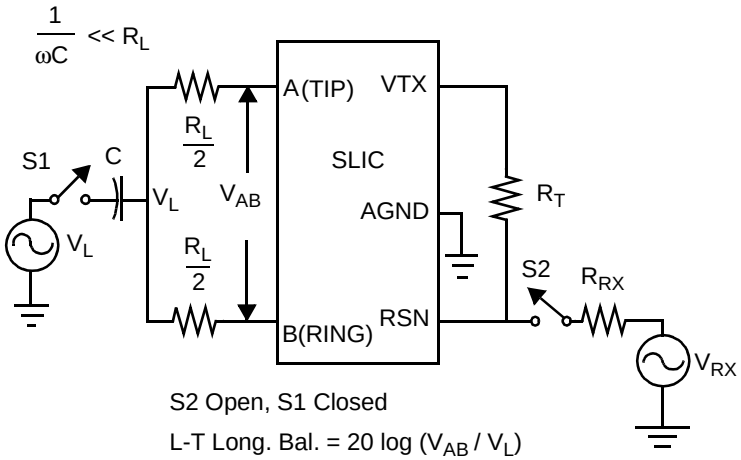
TEST CIRCUITS



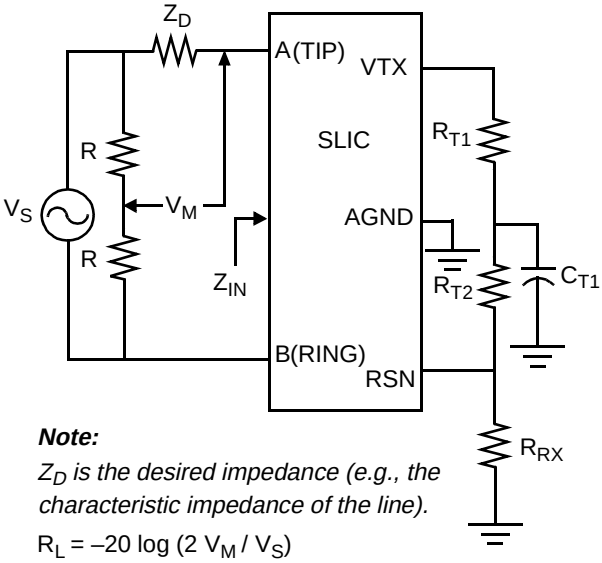
A. Two- to Four-Wire Insertion Loss



B. Four- to Two-Wire Insertion Loss and Balance Return Signal

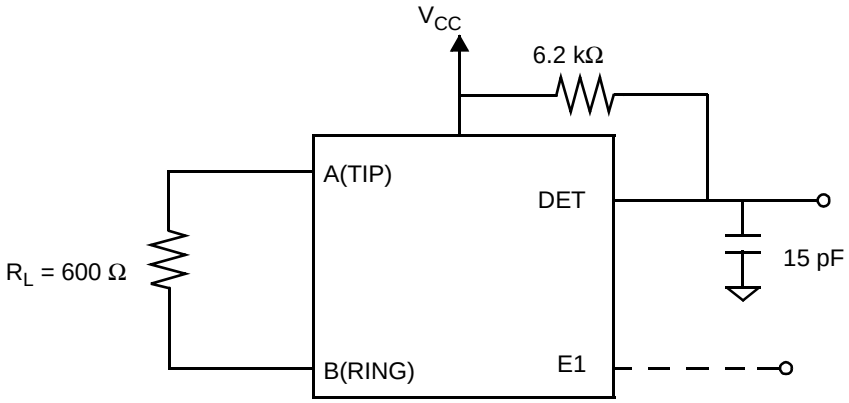


C. Longitudinal Balance

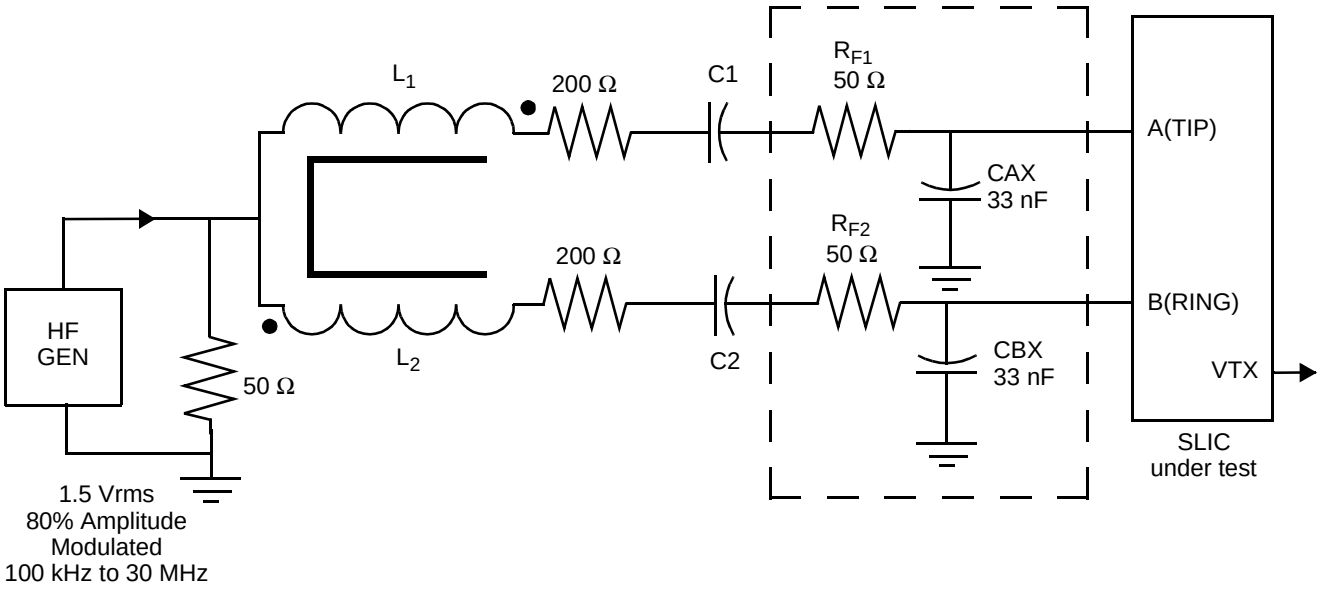


D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)

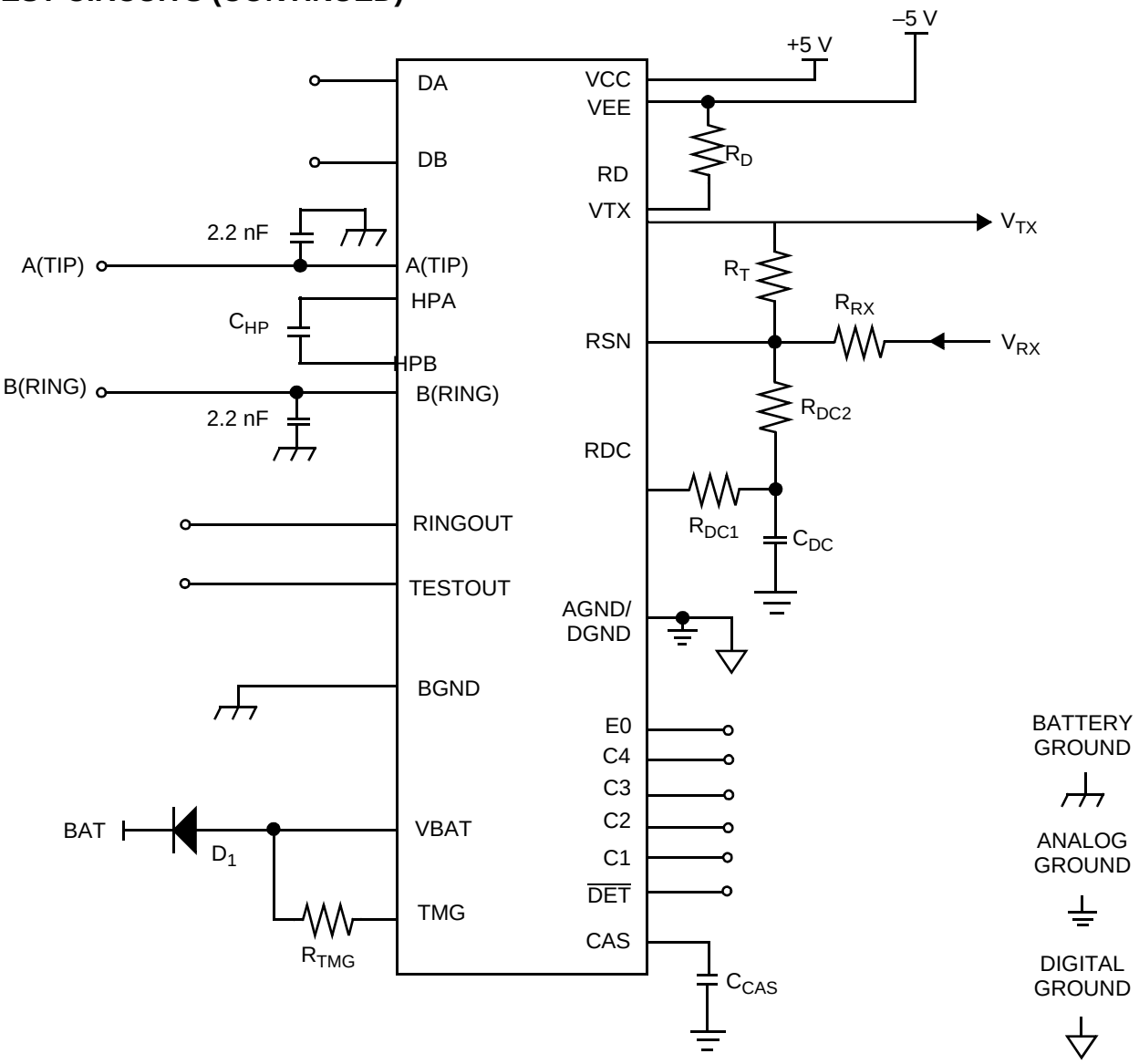


E. Loop-Detector Switching



F. RFI Test Circuit

TEST CIRCUITS (CONTINUED)



G. Am7947 Test Circuit

REVISION SUMMARY

Revision A to B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”
- Minor changes were made to the data sheet style and format to conform to AMD standards.